An Accurate Equivalent Circuit Model of Flip Chip and Via Interconnects

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Abstract— **In this paper, the transition discontinuities of flip chip circuits are modeled and investigated using finite-difference time-domain (FDTD) method to predict the S-parameters of different packages. This includes transition between two coplanar lines on the chip and mother board and transition between two striplines in a package. The computed S-parameter of the flip chip package using the FDTD model are used to develop an equivalent circuit for the transition discontinuity over a wide frequency band. A general and accurate equivalent circuit model of the interconnect has been developed and presented. In this circuit model, a statistical analysis is used to compute the value of the circuit elements. Also, losses in the flip chip package are represented by a simple function versus frequency. These losses include substrate loss of the chip and the mother board due to excitation of surface wave and radiation loss due to the bump. Conductor and material substrate losses are not included in this circuit model. Good agreement has been obtained between the S-parameters of the FDTD model and the equivalent circuit model over a wide frequency band of up to 50 GHz. Furthermore, the effects of the bump dimensions on the equivalent circuit model has been also evaluated and presented. The results show important issues in the design of the flip chip interconnect. The bump dimensions can be used as impedance matching parameters to achieve minimum losses over a wide frequency band. The presented equivalent circuit model can be used in commercial circuit simulators to predict monolithic microwave/millimeter wave integrated circuit (MMIC) performance including the package.**

I. Introduction

FLIP CHIP is emerging as the lead technology in multichip module packages. Several chips can be mounted together to the mother board using flip chip technology to increase density, improve system performance, and reduce cost [1]–[6]. This packaging technique also allows combinations of active and passive devices, silicon and gallium arsenide, and probably analog and digital circuits in the same application. In microwave circuits applications, low cost, high density, and short transition interconnects are considered to be the main advantages of the flip chip technique. Transitions in a flip chip package involve the use of metallic bumps (or via holes) to transmit the signal between the mother board and the chip. These bumps represent the main discontinuity to the signal propagating on the line which results in partial loss, reflection and possibly distortion of the signal. All these issues need to be considered in the design of the flip chip package. In order to minimize the effect of the transition discontinuity on the overall package performance, the bump dimensions as well as the characteristic impedance of both chip and mother board should be analyzed and investigated. In general, the characteristic impedance of the mother board, the chip, and the interconnect should be matched together to minimize the reflection due to the transition discontinuity.

This work is mainly concerned with the analysis and characterization of the flip chip package discontinuities using FDTD method with the objective of developing an equivalent circuit model of the bump (or via) discontinuities over a broad frequency band. An equivalent circuit model of the flip chip discontinuity will be a helpful tool in using commercial monolithic microwave/millimeter wave integrated circuit (MMIC) simulators to predict the overall performance including the package. In the literature, few papers have been published on the equivalent of bump discontinuities [19]–[20]. However, the effects of the flip chip technique are not clear. To date, no effort has been reported on the optimization of bump dimensions to reduce reflection and losses of flip chip package. As mentioned above, bump dimensions are very important parameters, and they have major effects on the package performance. We investigated the effects of the bump dimensions on the circuit model. In our analysis, two flip chip package configurations are considered. The first configuration is the transition between two striplines (SL-SL) on a single substrate package as shown in Fig. 1(a). In the second configuration, transition between two coplanar waveguides (CPW's) is assumed, and is referred to as CPW–CPW transition shown in Fig. 1(b). CPW's are popular at the chip level, whereas, the SL's are very popular at the package and mother board levels. Section II of this paper presents a brief discussion of FDTD method used for analysis and modeling. This includes excitation source requirements and boundary condition treatment. The S-parameters are also discussed in this section. In Section III, a statistical analysis is used to develop an equivalent circuit model of flip chip interconnects. Numerical verification to our code is presented in Section IV-A. A detailed study of the effects of via (or bump) dimensions on the equivalent circuit for the stripline-to-stripline transition (SL-SL) is presented in Section IV-B. Effects of staggering the bumps (signal and ground bumps) as well as underfill material on the equivalent circuit model for coplanar-to-coplanar transition (CPW-CPW) have been

Manuscript received March 29, 1996.

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Publisher Item Identifier S 0018-9480(96)08527-4.

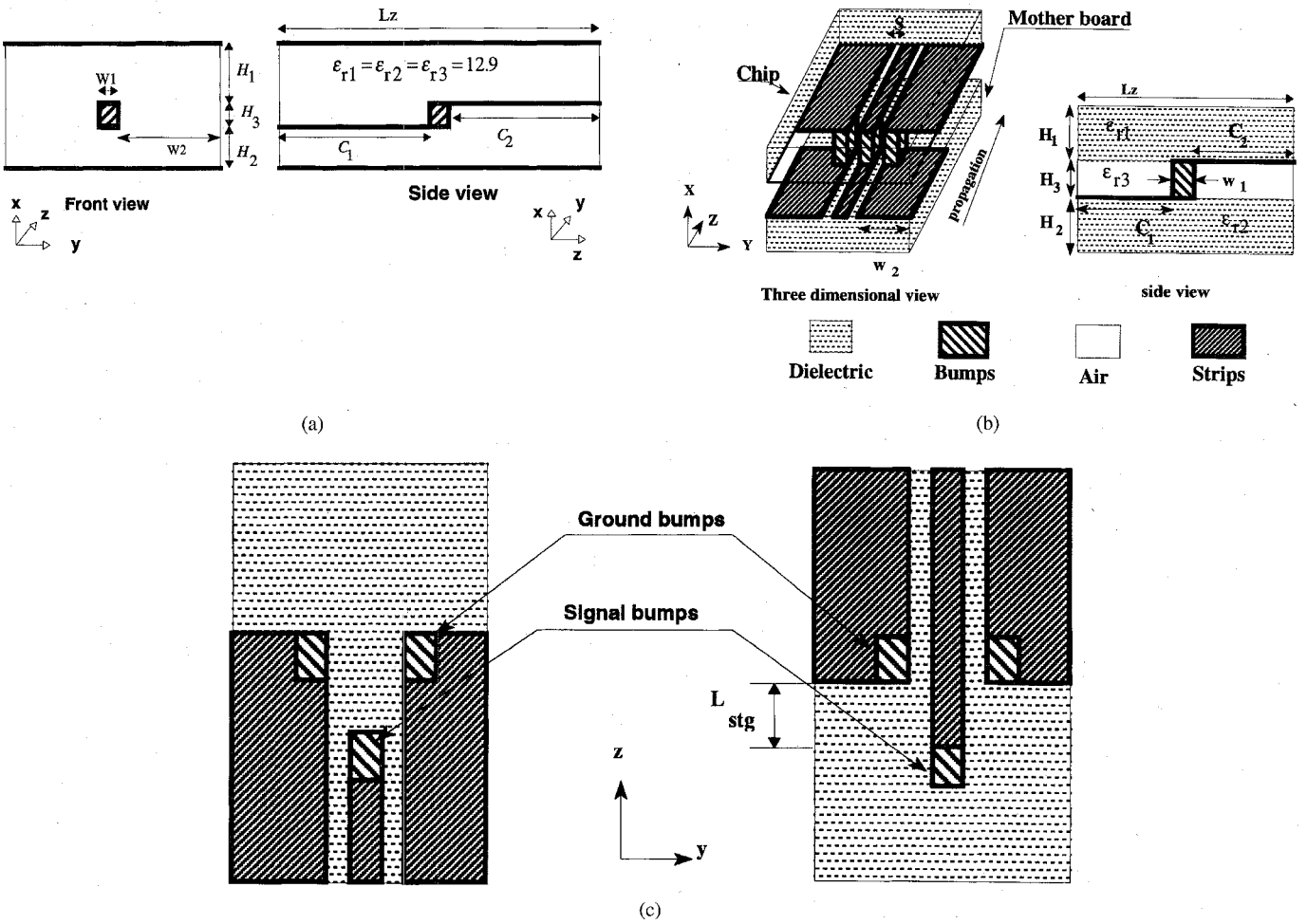


Fig. 1. Geometry of SL-SL, CPW-CPW (in-line) and staggered CPW-CPW transitions: (a) stripline package (SL-SL transition) $H_1 = H_2 = 0.36$ mm, $H_3 = 0.12$ mm, $W_1 = 0.24$ mm, $W_2 = 0.72$ mm, $C_1 = C_2 = 3.0$ mm, $L_z = 5.76$ mm, $\varepsilon_{r1} = \varepsilon_{r2} = \varepsilon_{r3} = 12.9$; (b) flip chip CPW with open termination (in-line basic configuration) $H_1 = H_2 = 0.36$ mm, $H_3 = 0.12$ mm, $W_1 = S = 0.12$ mm, $W_2 = 0.6$ mm, $C_1 = C_2 = 3.12$ mm, $L_z = 5.04$ mm, $\varepsilon_{r1} = \varepsilon_{r2} = 12.9, \varepsilon_{r3} = 1.0$; (c) flip chip CPW-CPW with staggered bumps (plan view of CPW-chip and CPW-mother board).

investigated and presented in Section IV-C. Results of S-parameters of the flip chip transitions as compared to the equivalent circuit model are also presented in Section IV, and Section-V concludes the present paper.

II. Finite-Difference Time-Domain Method

Finite-difference time-domain (FDTD) method is well known in principle since 1966 [7]. In microwave circuit applications, FDTD technique has been widely used in the analysis of microwave devices [8]–[10]. Recently, FDTD method has been effectively used to model the transition effects of high frequency interconnect in a flip chip package [11]–[13]. FDTD method is attractive due to its flexibility in handling a variety of circuits configurations. An additional benefit of the time-domain analysis is that a broad band pulse can be used as the excitation, and the frequency-domain response can be evaluated over a broad-band of frequencies by means of discrete Fourier transform of the transient response. In our analysis, we assume that media under consideration are uniform, isotropic, homogeneous and has no magnetic properties, i.e., $\mu_r \cong 1$. Furthermore, we assume that ground

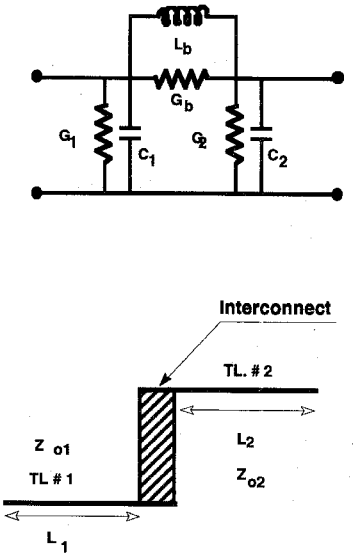
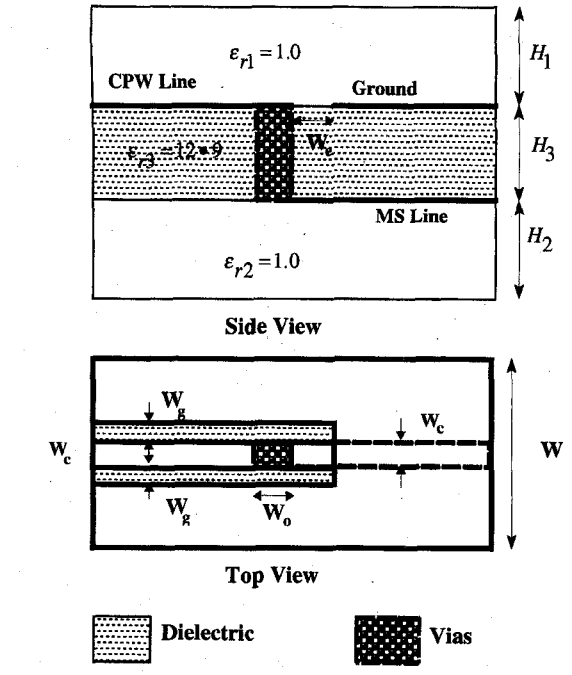
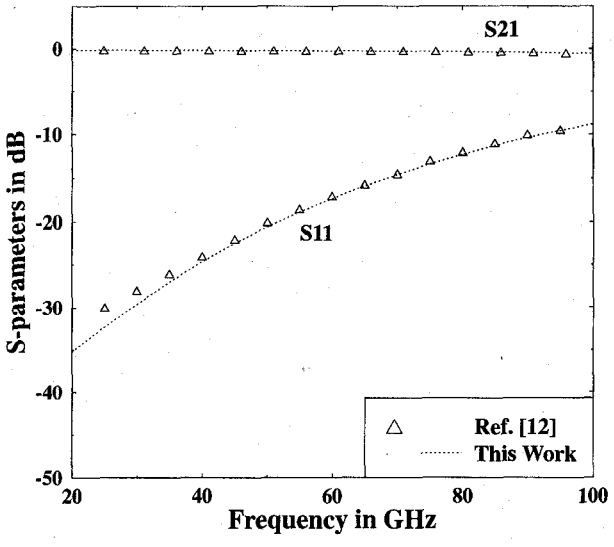


Fig. 2. Equivalent circuit model of the via (or bump).

and center conductors are perfect conductors (PEC) and have zero thickness. A gaussian pulse is used to modulate the



(a)



(b)

Fig. 3. (a) Geometry of MS-CPW transition of [12] (side and top views) $H_1 = H_2 = 0.4$ mm, $H_3 = 0.1$ mm, $W_g = 50$ μm, $W_c = W_o = 75$ μm, $W_e = 200$ μmm, $W = 1.0$ mm, $\varepsilon_{r1} = 1.0, \varepsilon_{r2} = 1.0, \varepsilon_{r3} = 12.9$. (b) S-parameters of MS-CPW transition of [12] compared to this work.

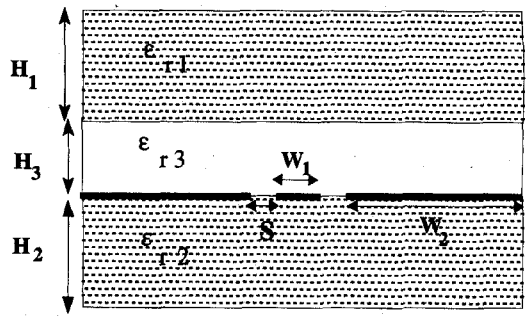
transverse spatial distribution of the excitation fields as

$$E_x(x,y) = \psi_x(x,y) \cdot \exp\big(-(t-t_0)^2/T^2\big) \quad (1)$$

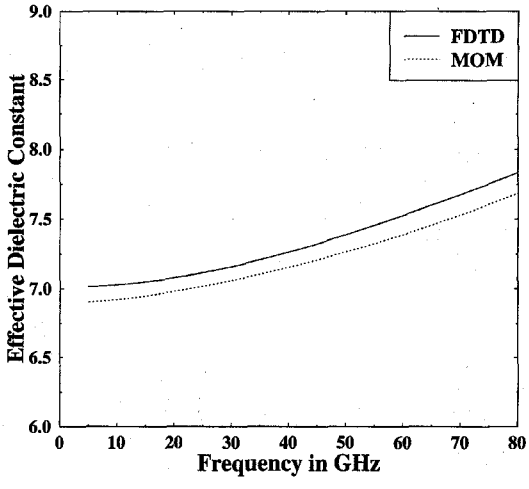
$$E_y(x,y) = \psi_y(x,y) \cdot \exp\big(-(t-t_0)^2/T^2\big) \quad (2)$$

where

- $\psi_x(x,y)$ the spatial distribution function for x-component of the electric field;
- $\psi_y(x,y)$ the spatial distribution function for y-component of the electric field;
- t_0 time center of the pulse;
- T pulse width.



(a)



(b)

Fig. 4. (a) Geometry of the cross section of the reference CPW structure (front view). $H_1 = H_2 = 0.36$ mm, $H_3 = 0.12$ mm, $W_1 = S = 0.12$ mm, $W_2 = 0.6$ mm, $\varepsilon_{r1} = \varepsilon_{r2} = 12.9, \varepsilon_{r3} = 1.0$. (b) Effective dielectric constant of the reference CPW structure using FDTD and MOM.

The spatial distribution functions, $\psi_x(x,y)$ and $\psi_y(x,y)$, are not initially known. However, a quasistatic TEM mode assumption can be used as an initial guess. In our analysis, a finite length section of a CPW line (or stripline) with the same cross section and dielectric layers as the flip chip package is used as reference structure. The objective of using this reference structure is to determine an accurate and well developed spatial distribution of the transverse electric field components (E_x and E_y) at the output. Then, this output, $\psi_x(x,y)$ and $\psi_y(x,y)$, is used at the source plane along with the gaussain pulse to excite the flip chip structures under investigation. In addition, the above CPW (or SL) structure is used as a reference in our calculations of the S-parameters of the flip chip package.

To simulate infinite structures, absorbing boundary conditions (ABC's) have to be added at the six outer walls of the computational domain. There are different techniques for simulating an ABC [14]–[17]. In our simulation, we used the super-absorption first-order Mur boundary conditions due to its simplicity and stability [14]–[15]. At the source plane, we apply the excitation field components (E_x and E_y) until the pulse is completely lunched, and then, switch to the ABC to avoid reflection from the source plane. Another boundary

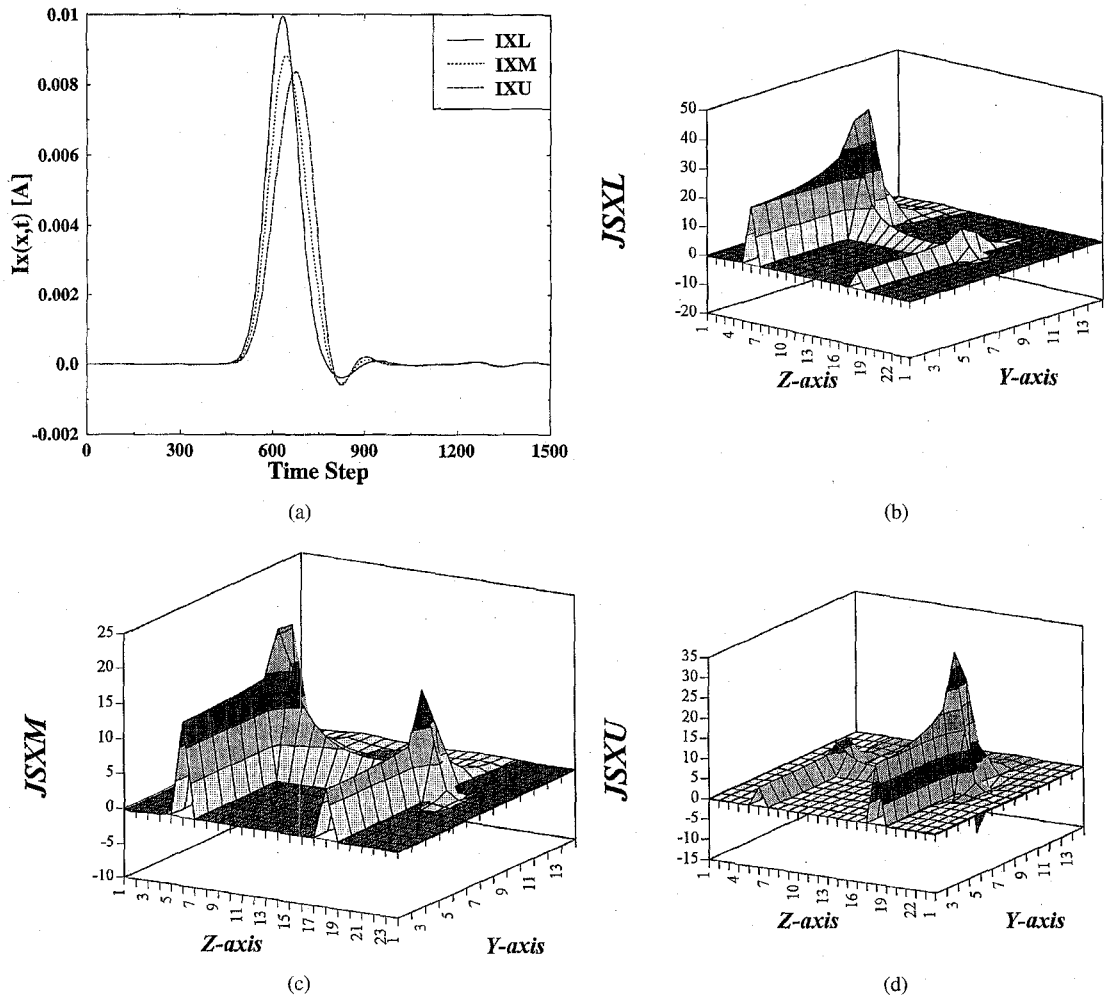


Fig. 5. (a) Total longitudinal current in the via direction $Ix(x,t)$ at three different cross sections versus time, IXL at $x = H_1$, IXM at $x = (H_1 + H_3/2)$ and IXU at $x = (H_1 + H_3)$. (b) Longitudinal current distribution at the bottom cross section of the via (JSXL). (c) Longitudinal current distribution at the middle cross section of the via (JSXM). (d) Longitudinal current distribution at the top cross section of the via (JSXU).

treatment (in case of CPW-CPW transition) is the air-dielectric interface where, the average dielectric constant is used, i.e., $(\varepsilon_1 + \varepsilon_2)/2$. Furthermore, in our simulation a technique of nonuniform mesh is used to reduce the memory requirement as well as to improve the accuracy of the results [18].

The effects of the flip chip interconnects can be characterized by evaluating the S-parameters. The S-parameters of a flip chip package are computed using FDTD as

$$S_{ij}(\omega) = \sqrt{-\frac{V_i^-(z_i,\omega)\cdot I_i^-(z_i,\omega)}{V_j^+(z_j,\omega)\cdot I_j^+(z_j,\omega)}} \tag{3}$$

where

V_i^- denotes the reflected voltage at the port (i);
V_j^+ denotes the incident voltage at the port (j);
I_i^- denotes the reflected current at the port (i);
I_j^+ denotes the incident current at the port (j);
ω denotes the angular frequency.

The above definition of S-parameters have been useful in reducing the numerical errors due to ABC to a secondary effect. (The voltage and current reflections due to ABC are out of phase.)

III. Equivalent Circuit Model

A general circuit model of a single transition interconnect is shown in Fig. 2. This model represents the transition interconnects between the chip and the mother board including losses. These losses include substrate loss and radiation loss. In general, substrate loss is due to the excitation of surface waves in the dielectric material, and it can be significant at high frequencies. The interconnect loss is due to radiation of the bump. In this model, the conductor and material losses have been neglected. The Y-parameters of the equivalent circuit model is given by

$$Y_{11}(\omega) = y_b(\omega) + y_1(\omega) \tag{4-a}$$
$$Y_{22}(\omega) = y_b(\omega) + y_2(\omega) \tag{4-b}$$
$$Y_{12}(\omega) = -y_b(\omega) \tag{4-c}$$
$$Y_{21}(\omega) = -y_b(\omega) \tag{4-d}$$

where

$$y_1(\omega) = G_1(\omega) + j\omega C_1 \tag{5-a}$$
$$y_2(\omega) = G_2(\omega) + j\omega C_2 \tag{5-b}$$
$$y_b(\omega) = G_b(\omega) + 1/j\omega L_b \tag{5-c}$$

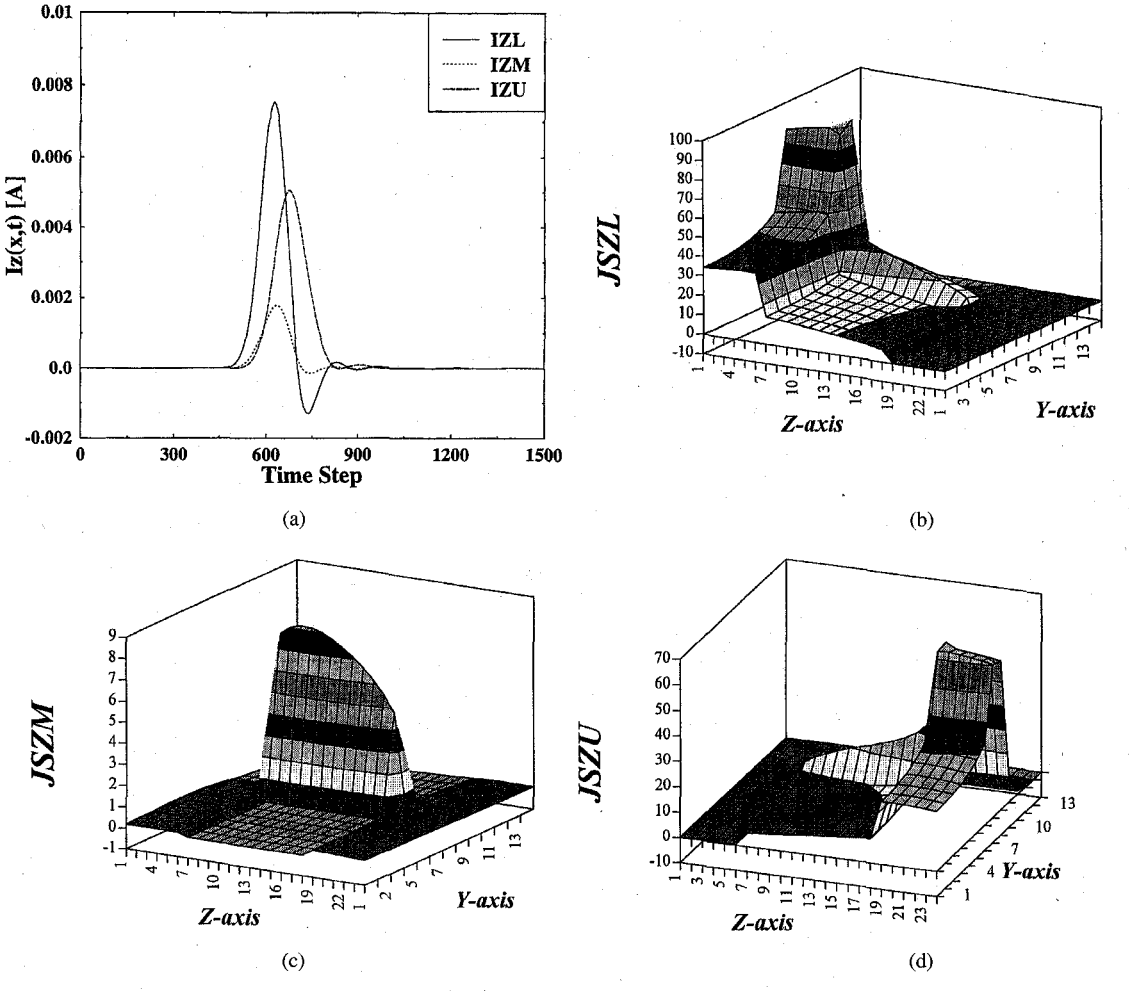


Fig. 6. (a) Total transverse current (normal) to the via direction $Iz(x,t)$ at three different cross sections versus time, IZL at $x = H_1$, IZM at $x = (H_1+H_3/2)$ and IZU at $x = (H_1 + H_3)$. (b) Transverse current distribution at the bottom cross section of the via (JSZL). (c) Transverse current distribution at the middle cross section of the via (JSZM). (d) Transverse current distribution at the top cross section of the via (JSZU).

where

- L_b denotes the inductance of the bump;
- G_b denotes the radiation conductance;
- C_1 denotes the discontinuity capacitance at the mother board;
- C_2 denotes the discontinuity capacitance at the chip;
- G_1 denotes substrate loss conductance of the mother board;
- G_2 denotes substrate loss conductance of the chip.

The radiation and substrate losses effects will be discussed in Section IV. To find the value of the above elements, a matching algorithm is used. In this algorithm the scattering parameters of the interconnects obtained from the FDTD are converted to the Y-parameters. The Y-parameters are then used to find the elements of the PI equivalent circuit using (4) and (5). A statistical analysis is used to find an average, or a simple function to approximately represent the frequency dependence. The following is the algorithm used to match the s-parameters of the circuit model.

1) Compute the mean value of the characteristic impedance of the reference structure line over the entire frequency band.

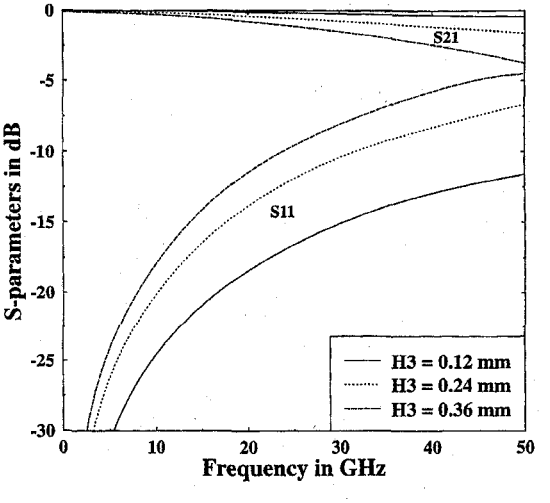


Fig. 7. S-parameters of SL-SL transition for different via heights.

2) Compute the mean values of the capacitance and the inductance over the entire frequency band.
3) Radiation conductance due to the bump is represented by $G_b(\omega) = K_b/f^2$, where K_b is constant computed as the mean value over the entire frequency band.

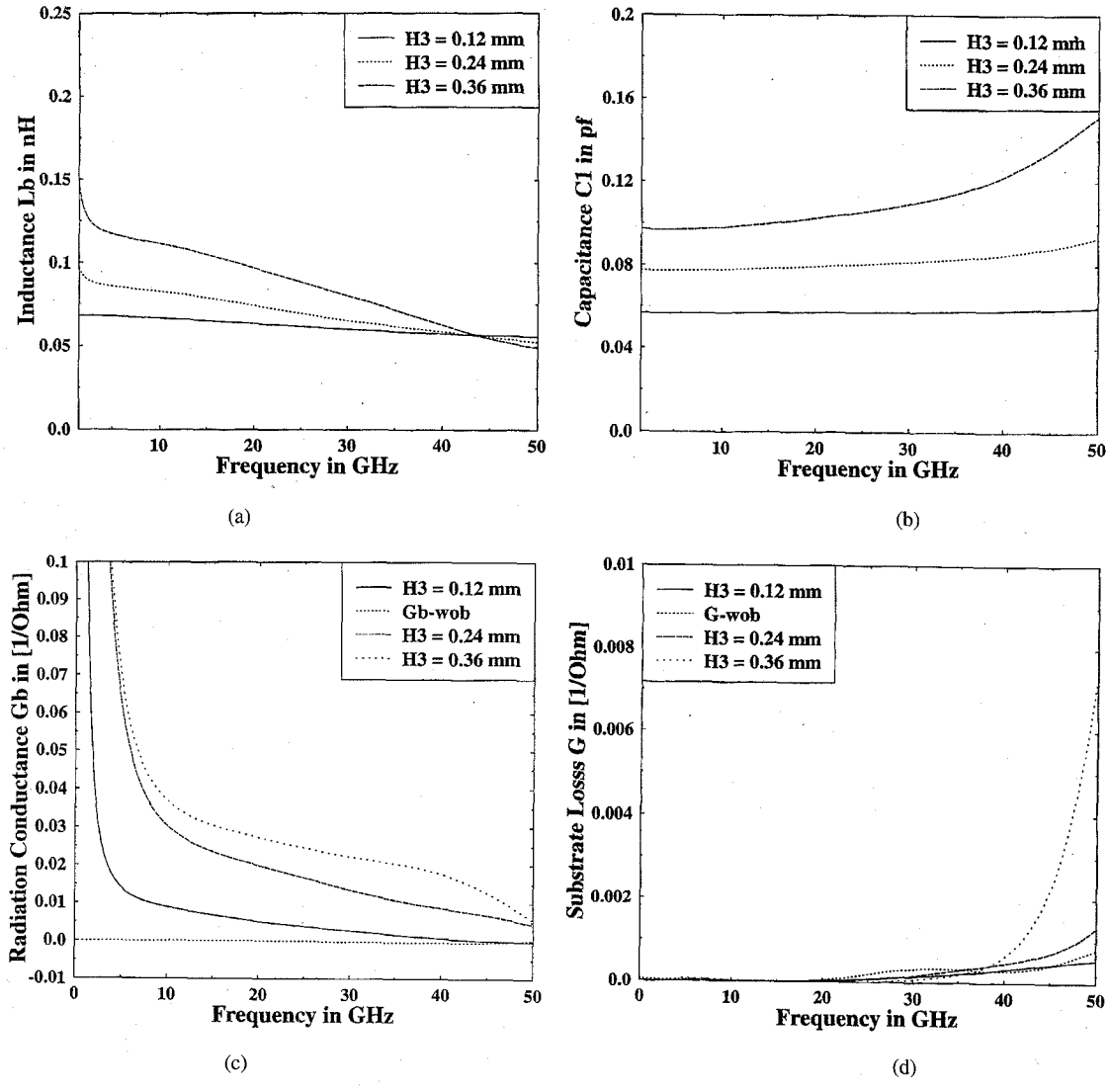


Fig. 8. Effects of via height on the elements of the equivalent circuit model (L_b, C_1, G_b, and G_1): (a) equivalent inductance L_b for different via heights; (b) equivalent capacitance C_1 for different via heights; (c) radiation conductance loss G_b versus via height and G_b-wob for $H_3 = 0.12$ mm; (d) substrate conductance loss G_1 versus via height and G-wob for $H_3 = 0.12$ mm.

4) Substrate loss conductance is approximated as

$$G_{1,2}(\omega) = K_{go1,2} \qquad f \le f_{o1,2}$$
$$= K_{go1,2} + K_{g1,2}(f - f_{o1,2})^2 \qquad f \ge f_{o1,2}$$

where

$G_{1,2}(\cdot)$	the substrate losses of the chip and mother board;
$K_{go1,2}$ and $K_{g1,2}$	constants computed for a broad band frequency response;
$f_{o1,2}$	the corner frequencies at which substrate losses of chip and mother board start to creep up.

Finally, the S-parameters of the circuit model are calculated using a circuit solver and compared to the FDTD parameters.

IV. Results

A. Numerical Verification

To verify our code, the transition investigated by [12], between a coplanar waveguide and a microstrip through a via on a single dielectric substrate [see Fig. 3(a)], is simulated using our code and is presented in Fig. 3(b). Excellent agreement

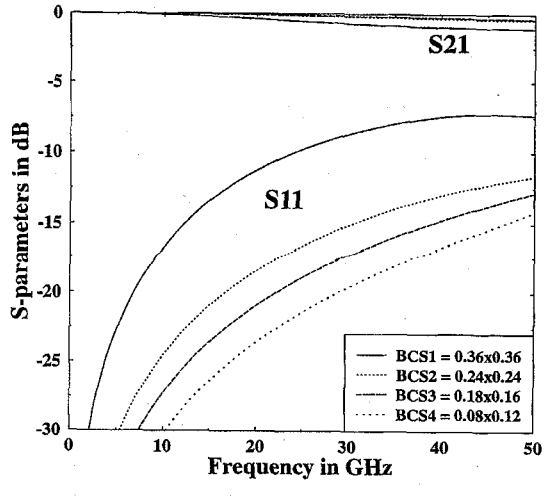


Fig. 9. S-parameters of SL-SL transition for different via cross section.

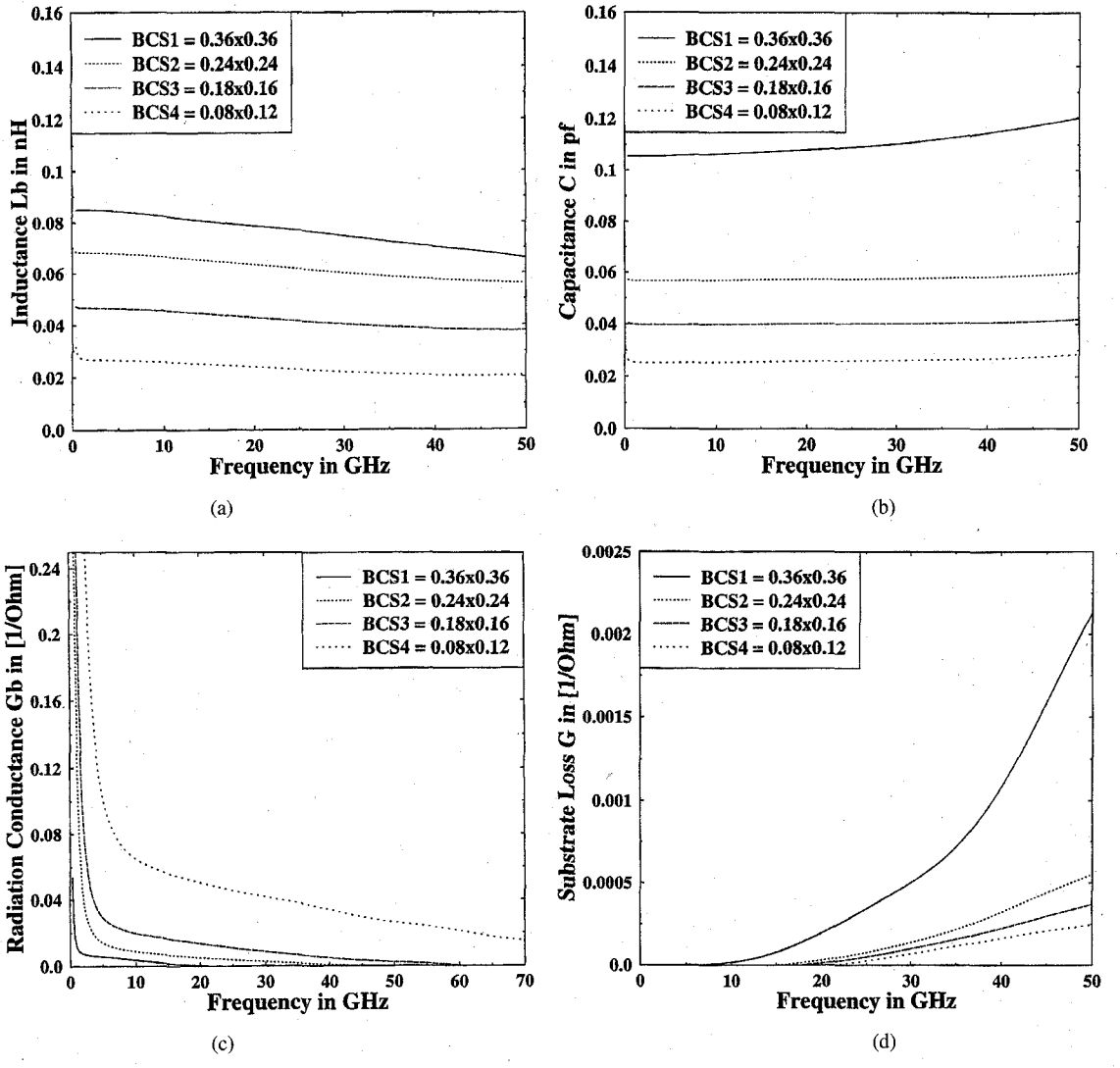


Fig. 10. Effects of the via cross section on the elements of the equivalent circuit model (L_b, C_1, G_b, and G_1): (a) equivalent inductance L_b for different via cross sections. (b) Equivalent capacitance C_1 for different via cross sections. (c) Radiation conductance loss G_b versus via cross section. (d) Substrate conductance loss G_1 versus via cross sections.

has been observed between our work and [12]. Further verification of our code was carried out by calculating the effective dielectric constant and the characteristic impedance of a reference multilayer CPW structure [see Fig. 4(a)] using both the method of moment and the FDTD method. Here, the effective dielectric constant is defined as $(\beta^2/\omega^2\mu_0\varepsilon_0)$. Excellent agreement has been obtained between the effective dielectric constants computed using the two methods as shown in Fig. 4(b). The computed characteristic impedance using either the moment method or the FDTD was approximately 50 ohms and varied very slightly over the entire band. Again, the difference between the two methods was negligible (less than 2%). In Section IV-C, this CPW structure will be used as a reference in our calculations of the S-parameters of CPW-CPW transition. Also, in case of SL-SL transition (Section IV-B), a stripline (SL) structure will be used as a reference for the calculations of the S-parameters as we explaned in Section II.

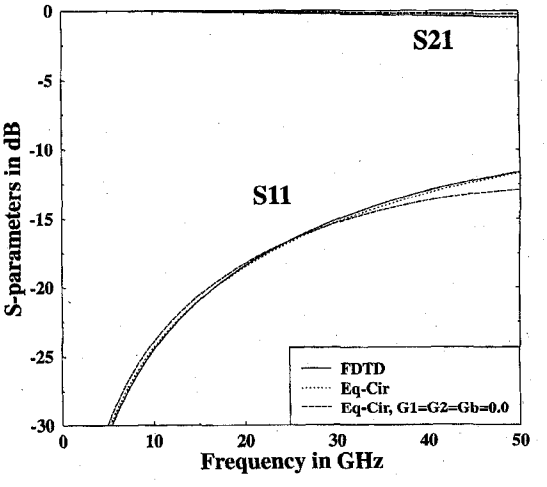


Fig. 11. S-parameters of flip chip SL-SL transition of both FDTD model and equivalent circuit model.

B. Results of SL-SL Circuit Model

To isolate the effects of bump transition from the effects of impedance mismatch and dielectric discontinuity, we have investigated the strip line transition through a via (Fig. 1(a)). This case also gives an insight on the effects of the geometry of a single via transition on the equivalent circuit shown in Fig. 2. As discussed above, FDTD is used to predict the S-parameters of the flip chip structure including a finite length of the transmission line (either CPW or stripline). This length must be subtracted to de-embed the via or the bump and to accurately evaluate the equivalent circuit of the transition. Therefore, an electrical reference of the via has to be determined. The reference can, in general, be at any point at the via, e.g., the center or the edge of the via. This reference can only be verified by studying the current distribution on the via surface.

The total current in the direction of the via $Ix(x,t)$ is shown in Fig. 5(a) at three different cross sections of the via versus time. This includes the current IXL at the lower cross section ($x = H_1$), the current IXM at middle cross section ($x = H_1 + H_3/2$), and the current IXU at upper cross section ($x = H_1 + H_3$). This figure also shows the time delay and dispersion of the pulse as it propagates in the via direction. The current distribution JSX(y,z) at same cross sections are also shown in the Fig. 5(b)–(d) (only half section of the via is shown). Here, the units of y-axis and z-axis are defined in terms of the number of FDTD cells assumed on half section of the via, where as the units of the vertical axis's are A/m. At the bottom ($x = H_1$) of the via, the surface current JSXL is mainly concentrated at the edge near the bottom stripline (Fig. 5(b)). At the middle cross section ($x = H_1 + H_3/2$, see Fig. 5(c)), the current JSXM on the opposite surface starts to increase and becomes dominant at the top surface (JSXU at $x = H_1 + H_3$) as shown in Fig. 5(d). This illustrates the current transition through the via between the bottom and the top striplines. We have also studied the transition of the transverse current between the striplines. The total current $Iz(x,t)$ in the transverse direction to the via (z-axis) is shown in Fig. 6(a) at the same cross sections mentioned above versus time. This figure also shows the time delay and the dispersion of the pulse as it propagates in the transverse direction to the via. Also, Fig. 6(b)–(d) shows the transverse current JSZ(y,z) at the three cross sections (JSZL, JSZM, and JSZU) of the via. Again, an edge inversion has been also observed in the transverse currents. The transverse currents become expectedly small at the middle of the via as shown in Fig. 6(a) and (c) (the transverse currents vanish at the edges and the via dimensions are very small). As in the longitudinal currents, the current flows from one edge at the bottom surface of the via to the opposite edge at the top surface of the via. Therefore, based on the current distributions of Figs. 5 and 6, we can conclude that the electrical reference of the via can be assumed at the edge. Consequently, the S-parameters of the via can be obtained by shifting the S-parameters of the flip chip structure to the via edges.

The effects of bump geometry on the equivalent circuit model are investigated and presented in Figs. 7–10. As the height of the via increase both insertion and reflection losses increase as shown in Fig. 7. Fig. 8(a) shows the equivalent inductance versus the via height. The inductance increases as the height increases especially at low frequencies, where the relation between the height and the inductance is almost linear. For small heights, the inductance is fairly flat versus frequency.

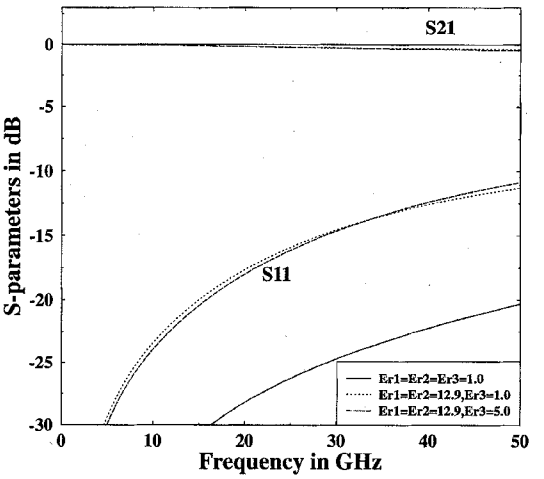


Fig. 12. S-parameters of the in-line CPW-CPW transition for different dielectric constants of the chip, mother board and underfill material.

As the height increases, the inductance decreases versus frequency and reflects the increased transmission line effects on the equivalent inductance. The discontinuity capacitance decreases as the height decreases as shown in Fig. 8(b) and should approach to zero when the via height goes to zero; i.e., no discontinuity is involved in the package. Fig. 8(c) shows the radiation conductance versus frequency for different via heights. The conductance decreases as $1/f^2$ similar to the radiation conductance of a short dipole. As the height of the via increases, the radiation conductance increases. This figure also includes the radiation conductance of the above geometry (for $H_3 = 0.12$ mm) with the via is physically removed. The conductance in this case is negligible compared to other cases where the via is present. This indicates that G_b is contributed by radiation from the via. The effects of the via height on the substrate conductance G_1 (or G_2) are shown in Fig. 8(d). In general, as the via height increases the substrate conductance increases. Again the conductance was plotted in the case where the via is removed (again for $H_3 = 0.12$ mm). A small change has been observed in G_1 or G_2 by the removal of the via indicating that this conductance is due to substrate loss at the line discontinuity. This type of loss remains very small before it starts to increase at a corner frequency f_0. This is shown in all cases of Fig. 8(d). Further discussions for this type of loss are introduced in Section IV-C.

Figs. 9 and 10 illustrate the effects of the via cross section on the the package performance. Fig. 9 shows that as the cross section of the via increases, the losses increase. The effect of line discontinuity on the equivalent circuit becomes more noticeable as the cross section increases. The values of $L_b, C, R_b(1/G_b), G_1$, and G_2 increase with increasing the cross section of the via as shown in Fig. 10(a)–(d). Finally, the results of the S-parameters of both equivalent circuit

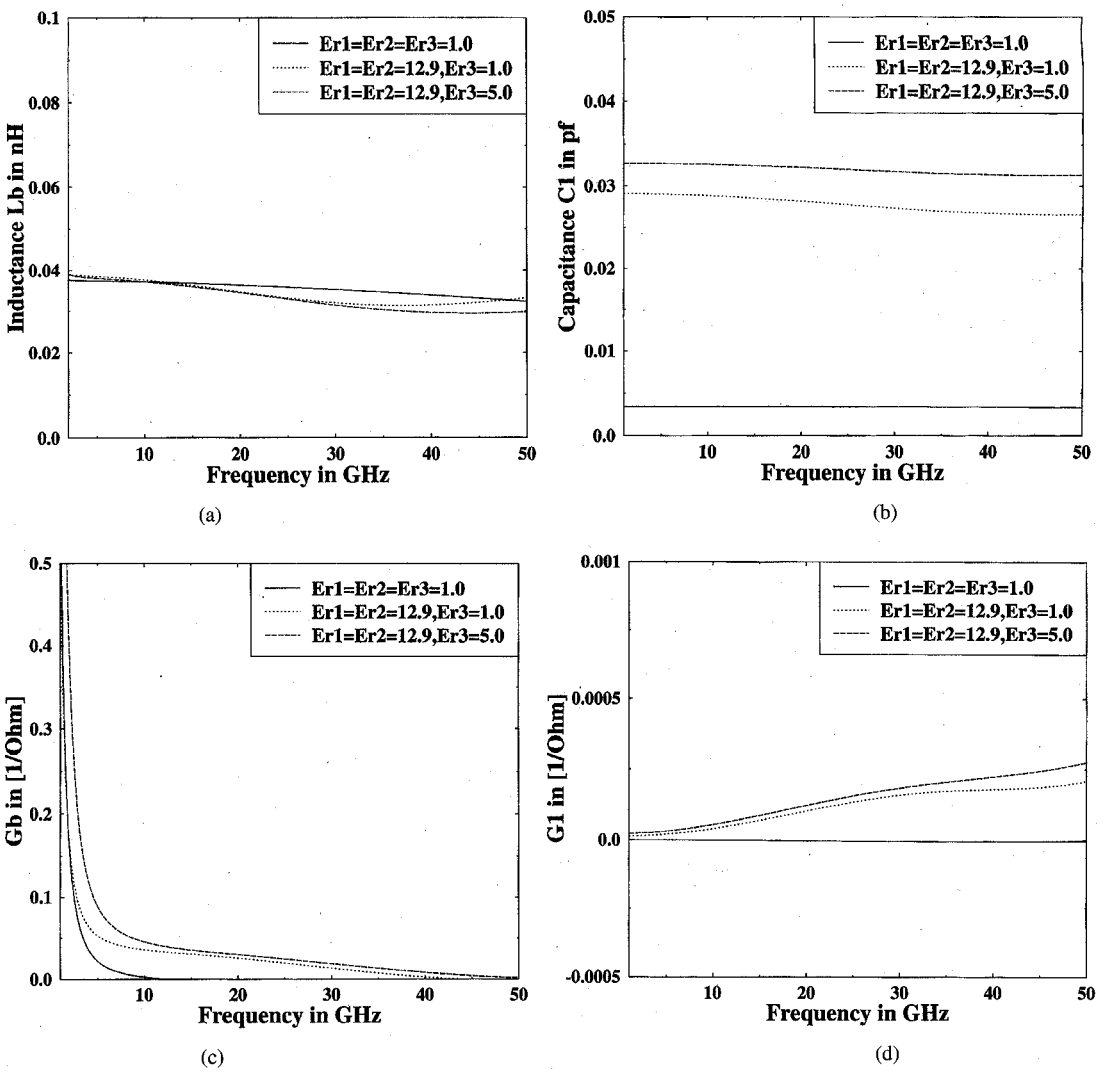


Fig. 13. Effects of the dielectric substrates (chip and mother board) and underfill material on the elements of the equivalent circuit model (L_b, C_1, G_b, and G_1): (a) equivalent inductance L_b; (b) equivalent capacitance C_1; (c) radiation conductance loss G_b; (d) substrate conductance loss G_1.

model and the FDTD model of the stripline package are shown in Fig. 11. The equivalent circuit model was verified and evaluated for a $0.24 \times 0.24 \times 0.12$ mm via using the technique described in Section III. Excellent agreement has been obtained up to 50 GHz between the S-parameters of both models. The difference in the computed $\mathbf{S_{11}}$ is less than 2% (less than 0.6 dB) over a wide frequency band (up to 50 GHz). For $\mathbf{S_{12}}$, the difference is less than 1% (less than 0.15 dB) up to 50 GHz. The difference between the equivalent circuit and the FDTD solutions will remain relatively small even whenlosses are neglected (G_1, G_2, and G_b are assumed to equal zero) as it is clear from Fig. 11.

C. Results of CPW-CPW Circuit Model

Equivalent circuit model of the CPW-CPW flip chip interconnect has been investigated in the case of in-line and staggered configurations (Fig. 1(b) and (c)). The S-parameters of in-line transition is shown in Fig. 12 versus frequency for different dielectric substrates and underfill material (the dielectric material between the two CPW lines). The lowest losses (S_{11} and S_{21}) have been obtained for low dielectric

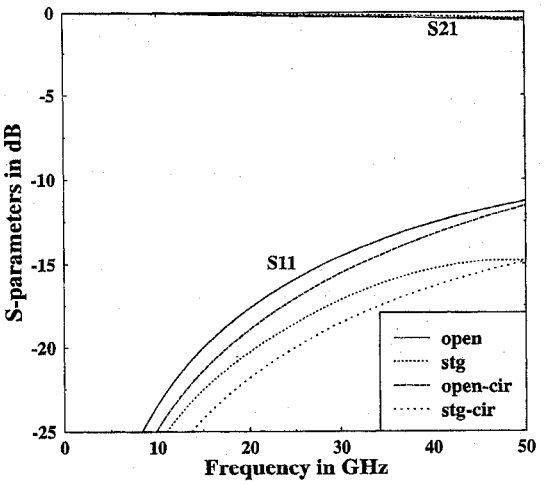


Fig. 14. S-parameters of open (in-line) and staggered CPW-CPW transitions for both FDTD model and equivalent circuit model.

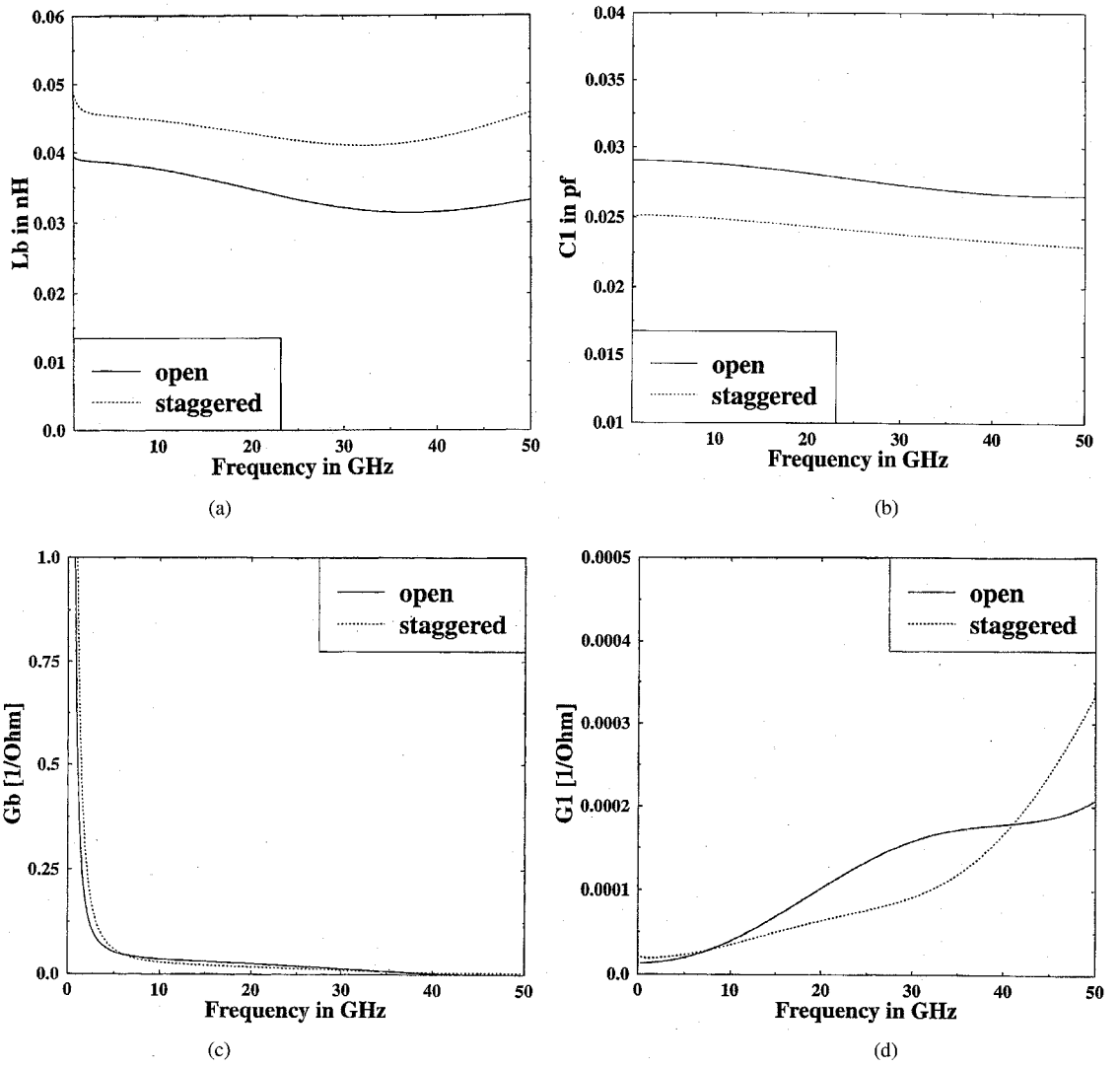


Fig. 15. Equivalent circuit elements (L_b, C_1, G_b, and G_1) of staggered versus open (in-line) CPW-CPW transitions: (a) equivalent inductance L_b of open versus staggered CPW-CPW transition; (b) equivalent capacitance C_1 of open versus staggered CPW-CPW transition; (c) radiation conductance loss G_b of open versus staggered CPW-CPW transition; (d) substrate conductance loss G_1 of open versus staggered CPW-CPW transition.

constants ($\varepsilon_{r1} = \varepsilon_{r2} = \varepsilon_{r3} = 1.0$.). Note that the effects of underfill material were not noticeable. As we expected, changing the dielectric constants should not have any effects on the equivalent inductance of the transition. This is shown in Fig. 13(a). However, the dielectric constant of the substrate is proportional to the equivalent capacitance of discontinuity as shown in Fig 13(b). There are also noticeable effects of the dielectric constants on the loss conductances G_b, G_1, and G_2 as shown in Fig. 13(c) and (d). It should be noted from Fig. 13(d), that when the dielectric constants of the chip, mother board and underfill material were set to unity ($\varepsilon_{r1} = \varepsilon_{r2} = \varepsilon_{r3} = 1.0$.), the substrate loss conductance G_1(or G_2) vanishes. This confirms the above conclusion that these conductances are mainly due to the substrate loss. The S-parameters of the circuit model is computed and compared to the FDTD results for the in-line (open) and staggered configurations for $0.12 \times 0.12 \times 0.12$ mm bumps and GaAs substrates ($\varepsilon_{r1} = \varepsilon_{r2} = 12.9$ and $\varepsilon_{r3} = 1.0$.). The results are presented in Fig. 14. As evident from the figure, a good agreement has been obtained up to 50 GHz between the S-parameters of both models. The difference in the computed $\mathbf{S_{11}}$ between the statistical and FDTD model is less than 6% (less than 1.5 dB) over a wide frequency band (up to 50 GHz). The difference in $\mathbf{S_{12}}$ is less than 2% (less than 0.5 dB) up to 50 GHz.

The effect of staggering the bumps on flip chip package performance using the electromagnetic model was explained in [13]. An optimum configuration of the staggered transitions to minimize losses were also investigated and presented in this reference. In this paper, using the equivalent circuit model, further investigation of the staggered design has been performed and presented in Fig. 15. This includes the effect of staggering the bumps on the capacitance and the inductance of the interconnects. Staggering the bumps decreases the capacitance (C_1 or C_2) and increases the inductance L_b of the transition (Fig. 15(a) and (b)). As a result, the characteristic impedance Z_0 of the interconnect is increased ($Z_0 = \sqrt{L_b/C}$) and approaches to 50 ohms which matches the characteristic impedance of the CPW lines. Consequently, reflections due to the bumps as well

as insertion loss is reduced. The effects of staggering the bumps on the conductance losses are predicted and presented in Fig. 15(c) and (d). Minor changes in G_b, G_1, and G_2 were observed when bumps are staggered. The agreement between the equivalent circuit model and FDTD model are still good for the staggered structure as shown in Fig. 14. However the agreement between the two models are not as good as in the case of in-line geometry. As in the case of the stripline package, we investigated the effects of neglecting the conductance losses (G_1, G_2 and G_b) on the circuit model. Minor effects on the frequency response of the equivalent circuit model has been predicted for both CPW-CPW transitions.

In addition to staggering the bumps, the interconnect dimensions (height and cross cestion) can be used as impedance matching parameters to achieve minimum losses. However, the minimum bump height is determined by the fabrication process, where as bump cross section is limited by the conductor width of the line. Therefore, the range over which the impedance can be controlled using the bump dimensions is also limited by the physical aspects of the package. Thus, staggering the bumps can be the lead alternative to minimize losses especially, when other techniques are not feasible.

V. Conclusion

A three-dimensional (3-D) finite difference time domain computer code has been developed to model and investigate the transition discontinuities in the flip chip package. The S-parameters based on the FDTD model along with the transition model are used to develop an equivalent circuit for the interconnect. Using a circuit solver, the equivalent circuit model of the flip chip package was verified versus the FDTD predictions over a broad band of frequencies. The minimum insertion and return loss of the package were found when the impedance of the transition discontinuity (via or bump) matches the line impedances. Effects of bump dimensions on the parameters that constitutes this impedance including inductance, capacitance, and conductances were studied in detail and presented. Staggering the bumps has been also found to be effective to control the impedance matching. The work presented in this paper significantly simplifies the simulation of a complex flip chip packages using the available circuit solvers. Future work will include investigation and modeling of the effects of conductor and material losses on the performance of flip chip package. Preliminary results indicate that, the contributions of these losses to the equivalent circuit are relatively small.

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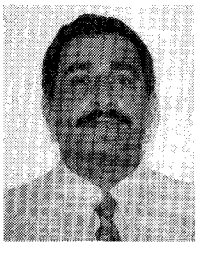

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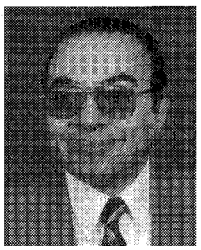

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